

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of forming a flash memory cell, comprising:

forming a tunnel oxide on a substrate;

forming a first conductor layer over the tunnel oxide;

forming an insulating layer over the first conductor layer, the insulating layer comprising a first oxide layer over the first conductor layer, a nitride layer over the first oxide layer, and a second oxide layer over the nitride layer, wherein the second oxide layer is formed by oxidizing said nitride layer with an ambient containing atomic oxygen;

forming a second conductor layer over the insulating layer;

etching at least the first conductor layer, the second conductor layer and the insulating layer, thereby defining at least one stacked gate structure; and

forming a source region and a drain region in the substrate on opposite side of said stacked gate structure, thereby forming at least one memory cell.

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2. The method of claim 1 wherein said second oxide layer is grown at a temperature of about 850°C to about 1100°C.

3. The method of claim 1 wherein said second oxide layer is grown at a temperature of less than about 900°C.

5 4. The method of claim 1 wherein said second oxide layer is grown for about 1 second to about 10 minutes.

5. The method of claim 1 wherein said second oxide layer is formed to at least about 60% of a targeted thickness.

10 6. The method of claim 1 wherein said atomic oxygen is supplied by in situ steam generation.

7. The method of claim 1 wherein said atomic oxygen is supplied by ozone source.

8. The method of claim 1 wherein said atomic oxygen is supplied by plasma source.

15 9. The method of claim 1 wherein said atomic oxygen is supplied by microwave source.

10. The method of claim 1 wherein said atomic oxygen is supplied by photoexcitation.

11. The method of claim 1 wherein said second oxide layer is formed in a single wafer system.

5 12. The method of claim 1 wherein said second oxide layer is formed in a batch furnace system.

13. The method of claim 1 wherein said second oxide layer is formed in a rapid thermal system.

10 14. The method of claim 1 wherein said second oxide layer is formed in a fast ramp system.

15 15. The method of claim 1 wherein said second oxide layer is formed to a thickness of about 20 Å - 80 Å.

16. A method of forming an ONO insulating structure comprising:

depositing a first oxide layer over an integrated circuit structure;

depositing a nitride layer over said first oxide layer; and

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growing a second oxide layer over said nitride layer wherein the second oxide layer is formed by oxidizing said nitride layer in the presence of atomic oxygen.

17. The method of claim 16 wherein said second oxide layer is grown at a temperature of about 850°C to about 1100°C.

18. The method of claim 16 wherein said second oxide layer is grown at a temperature of less than about 900°C.

19. The method of claim 16 wherein said second oxide layer is grown for about 1 second to about 10 minutes.

20. The method of claim 16 wherein said second oxide layer is formed to at least about 60% of a targeted thickness.

21. The method of claim 16 wherein said atomic oxygen is supplied by in situ steam generation.

22. The method of claim 16 wherein said atomic oxygen is supplied by ozone source.

23. The method of claim 16 wherein said atomic oxygen is supplied by plasma source.

24. The method of claim 16 wherein said atomic oxygen is supplied by microwave source.

5                    25. The method of claim 16 wherein said atomic oxygen is  
supplied by photoexcitation.

26. The method of claim 16 wherein said second oxide layer is formed in a single wafer system.

27. The method of claim 16 wherein said second oxide layer is  
10 formed in a batch furnace system.

28. The method of claim 16 wherein said second oxide layer is formed in a rapid thermal system.

29. The method of claim 16 wherein said second oxide layer is formed in a fast ramp system.

15 30. The method of claim 16 wherein said second oxide layer is  
formed to a thickness of about 20 Å - 80 Å.

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31. A method of forming a flash memory array containing a plurality of flash memory cells, each of said plurality of flash memory cells being formed by the acts of:

forming a tunnel oxide on a substrate;

5 forming a first conductor layer over the tunnel oxide;

forming an insulating layer over the first conductor layer, the insulating layer comprising a first oxide layer over the first conductor layer, a nitride layer over the first oxide layer, and a second oxide layer over the nitride layer, wherein the second oxide layer is formed by oxidizing said nitride layer in the presence of atomic oxygen;

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forming a second conductor layer over the insulating layer;

etching at least the first conductor layer, the second conductor layer and the insulating layer, thereby defining at least one stacked gate structure; and

15 forming a source region and a drain region in the substrate, thereby forming at least one memory cell.

32. The method of claim 31 wherein said second oxide layer is grown at a temperature of about 850°C to about 1100°C.

33. The method of claim 31 wherein said second oxide layer is grown at a temperature of less than about 900°C.

5 34. The method of claim 31 wherein said second oxide layer is grown for about 1 second to about 10 minutes.

35. The method of claim 31 wherein said second oxide layer is formed to at least about 60% of a targeted thickness.

10 36. The method of claim 31 wherein said atomic oxygen is supplied by in situ steam generation.

37. The method of claim 31 wherein said atomic oxygen is supplied by ozone source.

38. The method of claim 31 wherein said atomic oxygen is supplied by plasma source.

15 39. The method of claim 31 wherein said atomic oxygen is supplied by microwave source.

40. The method of claim 31 wherein said atomic oxygen is supplied by photoexcitation.

41. The method of claim 31 wherein said second oxide layer is formed in a single wafer system.

5 42. The method of claim 31 wherein said second oxide layer is formed in a batch furnace system.

43. The method of claim 31 wherein said second oxide layer is formed in a rapid thermal system.

10 44. The method of claim 31 wherein said second oxide layer is formed in a fast ramp system.

45. The method of claim 31 wherein said second oxide layer is formed to a thickness of about 20 Å - 80 Å.

46. A flash memory cell comprising:

a gate structure comprising:

15 a tunnel oxide on a substrate;

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a first conductor layer over the tunnel oxide;

an insulating layer over the first conductor layer, the insulating layer comprising a first oxide layer over the first conductor layer, a nitride layer over the first oxide layer, and a second oxide layer over the nitride layer, wherein the second oxide layer has a composition formed by the oxidation of said nitride layer in the presence of atomic oxygen;

~~a second conductor layer over the insulating layer; and~~

a source region and a drain region in the substrate on opposite sides of said gate structure.

47. The memory cell of claim 46 wherein said second oxide layer is formed to a thickness of about 20 Å - 80 Å.

48. A memory device comprising:

a flash memory array containing a plurality of flash memory cells, each of said plurality of flash memory cells comprising:

a gate structure comprising:

a tunnel oxide on a substrate;

a first conductor layer over the tunnel oxide;

an insulating layer over the first conductor layer, the insulating layer comprising a first oxide layer over the first conductor layer, a nitride layer over the first oxide layer, and a second oxide layer over the nitride layer, wherein the second oxide layer having a composition formed by the oxidation of said nitride layer in the presence of atomic oxygen;

a second conductor layer over the insulating layer; and

a source region and a drain region in the substrate on opposite sides of said gate structure.

49. The memory device of claim 48 wherein said second oxide layer is formed to a thickness of about 20 Å - 80 Å.

50. A processor based system comprising:

a central processing unit;

a memory device coupled to said central processing unit to receive data from and supply data to said central processing unit, said memory device having a flash memory cell comprising:

a gate structure comprising:

a tunnel oxide on a substrate;

a first conductor layer over the tunnel oxide;

5 an insulating layer over the first conductor layer, the insulating layer comprising a first oxide layer over the first conductor layer, a nitride layer over the first oxide layer, and a second oxide layer over the nitride layer, wherein the second oxide layer having a composition formed by the oxidation of said nitride layer in the presence of atomic oxygen;

a second conductor layer over the insulating layer; and

10 a source region and a drain region in the substrate on opposite sides of said gate structure.

51. The system of claim 50 wherein said second oxide layer is formed to a thickness of about 20 Å - 80 Å.